DECLARATION FOR PATENT APPLICATION
WITH POWER OF ATTORNEY

#3

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled *SPECTRALLY EFFICIENT FQPSK, FGMSK AND FQAM FOR ENHANCED PERFORMANCE CDMA, TDMA, GSM, OFDM AND OTHER SYSTEMS* the specification of which

(check one)

[ ] is attached hereto.

[X] was filed on August 9, 1999
Application Serial No. 09/370,360
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent Office all information known to me to be material to patentability as defined in 37 C.F.R. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes ☐	No ☐
(Number)	(Country)	(Day/Month/Year Filed)	Yes ☐	No ☐
(Number)	(Country)	(Day/Month/Year Filed)	Yes ☐	No ☐

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose to the Patent Office all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status)

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional applications listed below:

60/095,943	August 10, 1998
(Application Serial No.)	(Filing Date)

File No. A-66732-2/RMA

I hereby appoint the following attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Harold C. Hohbach, Reg. No. 17,757; Aldo J. Test, Reg. No. 18,048; Thomas O. Herbert, Reg. No. 18,612; Donald N. MacIntosh, Reg. No. 20,316; Edward S. Wright, Reg. No. 24,903; David J. Brezner, Reg. No. 24,774; Richard E. Backus, Reg. No. 22,701; James A. Sheridan, Reg. No. 25,435; Robert B. Chickering, Reg. No. 24,286; Richard F. Trecartin, Reg. No. 31,801; Steven F. Caserza, Reg. No. 29,780; Laura L. Kulhanjian, Reg. No. 33,257; Michael A. Kaufman, Reg. No. 32,988; Janet E. Muller, Reg. No. 35,294; Edward N. Bachand, Reg. No. 37,085; R. Michael Ananian, Reg. No. 35,050; Stephen M. Knauer, Reg. No. 38,208; Robin M. Silva, Reg. No. 38,304; David C. Ashby, Reg. No. 36,432; Maria S. Swiatek, Reg. No. 37,244; Steven M. Freeland, Reg. No. 42,555; William E. Nuttle, Reg. No. 42,943; Joseph Lutz, Reg. No. 43,765, provided that if any one of said attorneys ceases being affiliated with the law firm of Flehr, Hohbach, Test, Albritton & Herbert as partner, employee or of counsel, such attorney's appointment as attorney and all powers derived therefrom shall terminate on the date such attorney ceases being so affiliated.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, §1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first or sole Inventor: KAMILO FEHER

Inventor's signature: Kamilo Feher

Date: September 24, 1999

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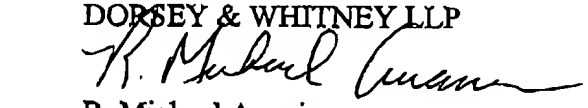
REMARKS

In response to the telephonic communication from the Publications Branch on 10 September 2002, applicant provides the requested brief description of FIGs. 10b, 11b, 11c, 13b, and 13c. This information is submitted in the form of an amendment, finds support in the application as filed and introduces no new matter.

Respectfully submitted,

DORSEY & WHITNEY LLP



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VERSION SHOWING CHANGES

FIG. 10b shows the implementation architecture of an alternative XCSI with PL single or multiple XCSI and/or Peak Limiter (PL) processor.

FIG. 11a illustrates NRZ signal and shaped Feher Return-to-Zero (FRZ) signal patterns and an embodiment having TCS response and cascade LR filters in which the LR filter is implemented with digital IIR and/or FIR filters.

FIG. 11b shows a pre-processor based architecture of a BRA system with single or multiple Signal Element (SE) storage and/or inverter and of single or multiple D/A based architecture having selectable 1 to N filter channel banks.

FIG. 11c shows an implementation of a Bit Rate Agile (BRA) pre-processor with single or multiple wavelets Signal Element (SE) storage and/or inverter and of filtered SE and ACM processors is illustrated.

FIG. 12a shows analog implementation components for cross-correlated and/or TCS-filtered data patterns and signals for bit rate agile and for high bit rate applications are shown.

FIG. 12b shows an analog BRA baseband implementation alternative of a TCS response processor for cross-correlated or not cross-correlated I and Q signals with selection or combined cascaded LR filter embodiment of this invention.

FIG. 13a is a mixed analog and digital circuit implementation alternative of this cross-correlated TCS response processor in cascade with LR filters.

FIG. 13b shows an other cross-correlated alternative implemented with a combination and/or selection of analog and digital circuits.

FIG. 13c shows a detailed implementation structure for one of the channels (I or Q) of a TCS response processor in cascade with a LR filter. In some embodiments the TCS processor contains cross-correlation between the I and Q channels while in other implementations there is no cross-correlation between the TCS response and cascaded LR filtered signals.